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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,780	11/19/2003	Byung-Jun Park	5649-948DV	6170

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EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,780	PARK, BYUNG-JUN	
	Examiner	Art Unit	
	Thinh T Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/172,760.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Claims 1-13 are pending in the Application.

Specification

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b/e) that form the basis for the rejections under this section made in this office action.

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim Rejections - 35 USC § 103

4. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-4,6-10,12-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (U.S. Patent 6,372,571) or as an alternative are rejected under 35 U.S.C. 103(a) as being obvious under Kim (US patent 6,372,571).

REGARDING CLAIM 1

Kim discloses a structure of an integrated circuit (fig 2, fig 5,fig 8,fig 9) comprising: conductive patterns (fig 8 layer 122) formed on a semiconductor substrate (fig 8 reference 100); dielectric patterns (fig 8 layer 134) disposed between the conductive patterns on the substrate, each having a cross-section with an upside-down T (fig 8 layer 134) shape and having greater thickness than the conductive patterns; a nitride film liner (fig 5 layer 126, column 6 line 19-20) lining trenches defined by the conductive patterns and the dielectric patterns; a dielectric layer (fig 5 layer 128, column 6 lines 17-18) on the nitride film liner, filling the trenches; and at least one metal contact plug (fig 9 reference 136) passing through the dielectric layer and the nitride film liner and in contact with at least one of the conductive patterns.

REGARDING CLAIM 2

Kim discloses a structure of an integrated circuit (fig 2, fig 5,fig 8,fig 9) further comprising first and second gates (fig 2 layer 110) and first and second sources/drains (fig 2 reference 113,113 a; 113b) a lower dielectric layer (fig 2 layer 116) formed on the first and second gates and the first and second sources/drains; and first and second contact plugs each in

contact with the first gate and the second source/drain, respectively, wherein the conductive patterns contact the upper surfaces of the first and second contact plugs.

REGARDING CLAIM 3,10

Kim discloses a structure of an integrated circuit (fig 2, fig 5,fig 8,fig 9) wherein the conductive patterns are bit-line stud pads (fig 9 layer 118).

REGARDING CLAIM 4,

Kim discloses a structure of an integrated circuit (fig 2, fig 4, fig 5,fig 8,fig 9) wherein the conductive patterns (fig 4 layer 122) are disposed in a peripheral circuit domain (the logic area A in Kim 's word) of the semiconductor substrate.

REGARDING CLAIM 6,13

Kim discloses a structure of an integrated circuit (fig 2, fig 4, fig 5,fig 8,fig 9) further comprising a metal interconnection (fig 9 reference 132) in contact with the upper surface of the metal contact plug.

REGARDING CLAIM 7

Kim discloses a structure of an integrated circuit (fig 2, fig 5,fig 8,fig 9) comprising: conductive patterns (fig 8 layer 122) formed on a semiconductor substrate in first and second domains (domain A and B fig 2) ; dielectric patterns (fig 8,9 layer 134) disposed between the conductive patterns on the semiconductor substrate, each having a cross-section with an upside-down T shape and having a greater thickness than the conductive patterns; a nitride film liner (fig 5 layer 126) lining trenches defined by the conductive patterns and the dielectric patterns; a dielectric layer(fig 5 layer 128) in the second domain and filling the trenches; nitride film studs having insubstantial step difference with respect to the dielectric patterns on the first

domain, the nitride film studs covering the upper surfaces of the conductive patterns; at least one capacitor (fig 9 in area B) in contact with a conductive region of the semiconductor substrate and passing through the dielectric patterns; an intermetal dielectric layer on the capacitor and the dielectric layer; and at least one metal contact plug(fig 8 layer 132) in contact with at least one of the conductive patterns and passing through the intermetal dielectric layer, the dielectric layer and the nitride film liner.

REGARDING CLAIM 8

Kim discloses a structure of an integrated circuit (fig 2, fig 4, fig 5,fig 8,fig 9) wherein the first domain (domain B) is a cell domain and the second domain (domain A) is a peripheral circuit domain.

REGARDING CLAIM 9

Kim discloses a structure of an integrated circuit (fig 2, fig 4, fig 5,fig 8,fig 9) comprising: first and second gates and first and second sources/drains each formed in the second domain (fig 9, region A logical peripheral area) ; a plurality of third gates and a plurality of third sources/drains in the first domain (fig 9; region B cells area) a lower dielectric layer formed on the first, second and third gates and the first, second and third sources/drains; first and second conductive pads formed within the lower dielectric layer and contacting a plurality of third source/drains; and first, second and third contact plugs passing through the lower dielectric layer and in contact with upper surfaces of the first gate, wherein the conductive pads contact the upper surfaces of the first, second and third contact plugs, and the conductive region includes the upper surface of the first conductive pad.

Claim Rejections - 35 USC § 103

6. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US patent 6,372,571) in view of further remark.

REGARDING CLAIM 5,11

Kim (fig 2, fig 4, fig 5,fig 8,fig 9) discloses all the invention except is silent about the range of the thickness of the nitride film liner. However, it has been held that where the general conditions of a claim are disclosed in prior art discovering the optimum or workable range involves only routine skill in the art.

8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

10. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) in the parent application 10/172,760 which papers have been placed of record in the file.

CONCLUSION

11. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Liaw (US patent 6,448,140) discloses a Laterally recessed tungsten silicide gate structure used with a self-aligned contact structure including a straight walled sidewall spacer while filling recess, Deboer et al. (US patent 6,365,453) disclose a method and structure for reducing contact aspect ratio.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen TTN

Art Unit 2818

David Nelms
Supervisory Patent Examiner
Technology Center 2800